Global DC-Analysis with the Aid of Standard Network Analysis Programs

Tobias Nähring* and Albrecht Reibiger**

Technische Universität Dresden, Germany

Abstract. We present applications of homotopy methods, which make it possible to compute multiple dc-operating points of transistor circuits with standard network analysis programs. It is possible to capture all dc-operating points at least of smaller transistor networks with the help of one- and two-parametric homotopies. Uniqueness criteria of network theory can help to find a parameterization of the homotopy path. As an example for appropriate uniqueness criteria a well known theorem of Nielsen and Willson is applied. Bounds for the parameter space can be found by the no-gain property of transistor circuits.

1 Introduction

Most of the standard network analysis programs are provided with some Newton Raphson like algorithm for dc-analysis computing just one dc-operating point (e. g. Newton Raphson algorithm with source stepping). But often it is important to know whether a circuit can exhibit other dc-operating points than the computed one. The reader is reminded only of the unwanted latch-up effect of the operational amplifier μA709 (see [2]).

In [8] new classes of homotopy methods for the computation of multiple dc-operating points have been introduced which can be realized by means of standard network analysis programs. Here we give a short review of the driving-point-characteristic method (dpc-method), discuss its feasibility, and show some applications in greater detail.

2 Some network theoretic preliminaries

In this paper a transistor circuit is modeled as a resistive network $\mathcal{N}$. The topology of $\mathcal{N}$ is described by an oriented graph $\mathcal{G}$ with some branch set $\mathcal{Z}$ (e. g. one branch per resistor, two branches per transistor). Normalized voltage- and current assignments to the branches of $\mathcal{G}$ are the elements (v, i) of the set[1] $\mathcal{S} := \mathbb{R}^{\mathcal{Z}} \times \mathbb{R}^{\mathcal{Z}}$. The v-i-relation $\mathcal{V} \subseteq \mathcal{S}$ models the behavior of

* e-mail `naehring@iee.et.tu-dresden.de`

** e-mail `reibiger@iee.et.tu-dresden.de`

[1] An element $x \in \mathbb{R}^{\mathcal{Z}}$ assigns to each branch $b \in \mathcal{Z}$ a value $x_b \in \mathbb{R}$.

the devices contained in the circuit. It is most often described by equations. E. g., to model bipolar transistors we use the Ebers-Moll equations

$$i_c = I_{\mathrm{CS}}\,(\,\exp{(v_c/V_{\mathrm{T}})} - 1\,) - \alpha_{\mathrm{f}} I_{\mathrm{ES}}\,(\,\exp{(v_e/V_{\mathrm{T}})} - 1\,)\,,$$
$$i_e = I_{\mathrm{ES}}\,(\,\exp{(v_e/V_{\mathrm{T}})} - 1\,) - \alpha_{\mathrm{r}} I_{\mathrm{CS}}\,(\,\exp{(v_c/V_{\mathrm{T}})} - 1\,)$$

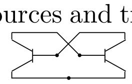
where e is the branch from base to emitter and c is the branch from base to collector, and where the constants $V_{\mathrm{T}}, I_{\mathrm{CS}}, I_{\mathrm{ES}}, \alpha_{\mathrm{f}}, \alpha_{\mathrm{r}}$ have the usual meaning.

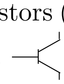
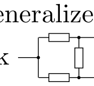
For a network $\mathcal{N}$ with graph $\mathcal{G}$ and v-i-relation $\mathcal{V}$ we write condensed $\mathcal{N} = (\mathcal{G}, \mathcal{V})$. The electrical junctions between the parts of the circuit are modeled by the graph $\mathcal{G}$ and the corresponding mesh and cutset equations. The set of voltage-current-assignments $(v, i) \in \mathcal{S}$ obeying Kirchhoff's laws is named Kirchhoff's set and denoted by $\mathcal{H}$. Finally, we have $\mathcal{L} := \mathcal{V} \cap \mathcal{H}$, the solution set of $\mathcal{N}$ which stands for the set of the dc-operating points of the entire circuit. With these notations the following two statements are direct consequences of set theory.

Intersection theorem: Let $\mathcal{N} = (\mathcal{G}, \mathcal{V})$, $\bar{\mathcal{N}} = (\mathcal{G}, \bar{\mathcal{V}})$, $\widetilde{\mathcal{N}} = (\mathcal{G}, \widetilde{\mathcal{V}})$ be networks with the same graph $\mathcal{G}$. If $\mathcal{V} = \bar{\mathcal{V}} \cap \widetilde{\mathcal{V}}$ then $\mathcal{L} = \bar{\mathcal{V}} \cap \widetilde{\mathcal{L}}$.

Covering theorem: Let $\mathcal{N} = (\mathcal{G}, \mathcal{V})$ be a network and $(\mathcal{N}^x)_{x \in X}$ a family of networks $\mathcal{N}^x = (\mathcal{G}, \mathcal{V}^x)$ with the same graph as $\mathcal{N}$. If $\mathcal{V} = \cup_{x \in X} \mathcal{V}^x$ then $\mathcal{L} = \cup_{x \in X} \mathcal{L}^x$.

Throughout this paper we assume that networks are connected and do not have cutsets of independent current sources or loops of independent voltage sources. The transistor models have the no-gain property (see [6]). So the absolut value of any branch voltage (current) of a solution of a network $\mathcal{N}$ does not exceed the sum of the absolut values of the voltages (currents) of the independent sources in $\mathcal{N}$.

Let $\mathcal{N}$ be a network consisting of resistors, independent voltage and current sources and transistors. We say that $\mathcal{N}$ is *reducible to the feedback structure* if  (the feedback structure) is a possible outcome of the following three-step algorithm:

1. choose two transistors (npn and/or pnp), replace them by the generalized transistor symbol , replace all others by the resistor network ,
2. choose some resistors and remove them; remove all current-sources,
3. contract[2] all voltage-source branches and all remaining resistor branches.

If $\mathcal{N}$ is not reducible to the feedback structure then $\mathcal{N}$ has at most one dc-operating point. This uniqueness statement is a consequence of the well known fundamental theorem of Nielsen and Willson for bipolar transistor networks (cf. [4]). We will utilise it in section 3.

In certain examples, where additional controlled sources were involved, the method of Hasler an Neirynck (see [7]) has been successfully employed as a replacement for the theorem of Nielsen and Willson.

[2] 'Contracting a branch' means identifying its incident nodes and removing it.

3 The dpc-method for the global dc-analysis of transistor circuits

In this section we introductorily describe an application of the dpc-method to the simple flip-flop network in figure 1.

For the analysis of this network an open circuit a is inserted which does not influence the solutions of the network. The so modified network $\mathcal{N} = (\mathcal{G}, \mathcal{V})$ is depicted in figure 2. As we will see below it is possible to determine all dc-operating points of $\mathcal{N}$ with the help of this additional branch.

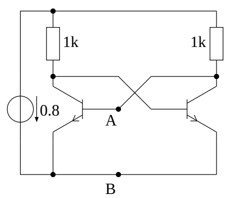


Figure 1

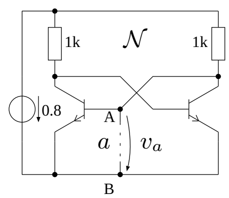


Figure 2

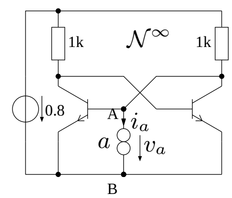


Figure 3

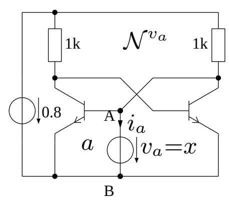


Figure 4

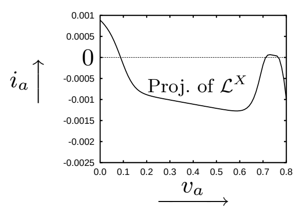


Figure 5

In this example the dpc-method is applied to the interconnection of the flip-flop network with the open circuit a at the terminals A and B.

The v-i-relation $\mathcal{V}$ of $\mathcal{N}$ is represented as the intersection $\mathcal{V} = \mathcal{V}^\infty \cap \mathcal{V}^0$ of the v-i-relations of two modified networks $\mathcal{N}^\infty$ and $\mathcal{N}^0$. The network $\mathcal{N}^\infty$ is constructed from $\mathcal{N}$ by replacing the open circuit by a norator[3] (cf. fig. 3), i.e. the equation $i_a = 0$ is removed from the system of behavioral equations for this network. In the system of defining equations for the solution set $\mathcal{L}^\infty$ of $\mathcal{N}^\infty$, the number of variables exceeds the number of equations by one. Thus, we expect that $\mathcal{L}^\infty \subset \mathcal{S}$ is an one-dimensional manifold. We will use a partial curve $\mathcal{L}^X \subset \mathcal{L}^\infty$ as homotopy path. The projection of $\mathcal{L}^X$ onto the (v_a, i_a)-plane is shown in figure 5.

The other network $\mathcal{N}^0$ results from $\mathcal{N}$ by exchanging all branches except the open circuit for norators. Thus, the only behavioral equation left for this network is the equation $i_a = 0$ and $\mathcal{V}^0$ is a hypersurface of the space $\mathcal{S}$.

[3] For norators all pairs of voltages and currents are admissible (see e. g. [7]).

With $\mathcal{V} = \mathcal{V}^\infty \cap \mathcal{V}^0$ the intersection theorem implies $\mathcal{L} = \mathcal{L}^\infty \cap \mathcal{V}^0$, i.e., the intersection points of $\mathcal{L}^\infty$ with the hypersurface $\mathcal{V}^0$ are the dc-operating points of $\mathcal{N}$. To find some of them we search the homotopy path $\mathcal{L}^X$.

The homotopy path can be computed via a dc-sweep of `spice`: For any $x \in \mathbb{R}$ let $\mathcal{N}^x = (G, \mathcal{V}^x)$ be the network that results from replacing the norator in $\mathcal{N}^\infty$ by a voltage source with source voltage x (see fig. 4). For $x \in \mathbb{R}$ the v-i-relation $\mathcal{V}^x$ of $\mathcal{N}^x$ differs only from $\mathcal{V}^\infty$ by the additional condition $v_a = x$ of the inserted voltage source and can therefore be written as $\mathcal{V}^x = \{(v,i) \in \mathcal{V}^\infty | v_a = x\}$. Thus, $\mathcal{V}^\infty = \cup_{x\in\mathbb{R}} \mathcal{V}^x$ and by the covering theorem we have $\mathcal{L}^\infty = \cup_{x\in\mathbb{R}} \mathcal{L}^x$. If for each $x \in \mathbb{R}$ the solution of the network $\mathcal{N}^x$ is unique (i.e., the solution set $\mathcal{L}^x$ has just one element), we obtain a map $x \in \mathbb{R} \mapsto (u,i) \in \mathcal{L}^x$ which parameterizes $\mathcal{L}^\infty$. Actually, this is the motivation for the insertion of a voltage source at the nodes A and B (review fig. 1 to 4). The inserted voltage source *breaks all feedback structures* of $\mathcal{N}$, i.e. the network $\mathcal{N}^x$ is not reducible to the feedback structure and the theorem of Nielsen and Willson ensures that the network $\mathcal{N}^x$ has a unique solution.

In general, it is only possible to compute a numerical approximation of a partial curve $\mathcal{L}^X := \cup_{x\in X} \mathcal{L}^x$ of $\mathcal{L}^\infty$ which is defined on a bounded parameter interval $X \subset \mathbb{R}$. Still we have $\mathcal{L}^X \cap \mathcal{V}^0 \subset \mathcal{L}^\infty \cap \mathcal{V}^0 = \mathcal{L}$ and therefore the intersection points of the homotopy path $\mathcal{L}^X$ with the hypersurface $\mathcal{V}^0$ are dc-operating points of $\mathcal{N}$. Since we want to find all dc-operating points of $\mathcal{N}$ we have to estimate bounds for the parameter interval X such that $\mathcal{L}^X$ contains all solutions of $\mathcal{N}$. Often, the no-gain property of transistor circuits can be applied for this task. Because of this property the branch voltages v_a of all solutions (v,i) of the network $\mathcal{N}$ cannot exceed the boundaries of the interval $[0, 0.8]$ which is determined by the voltage of the power supply[4]. Thus, with $X := [0, 0.8]$ the solutions of $\mathcal{N}$ are all contained in $\mathcal{L}^X$.

Often, more than one independent source is needed, to break all feedback structures of a transistor network. Let $\mathcal{N} = (G, \mathcal{V})$ be such a network and let $\bar{\mathcal{Z}}_V$ and $\bar{\mathcal{Z}}_I$ be minimal sets of branches in $\mathcal{N}$ that break all feedback structures of $\mathcal{N}$ if they are replaced by independent voltage and current sources, resp. Analogous to the introductory example we construct a network $\mathcal{N}^\infty$ by replacing all the branches in $\bar{\mathcal{Z}} := \bar{\mathcal{Z}}_V \cup \bar{\mathcal{Z}}_I$ for norators and a network $\mathcal{N}^0$ by replacing all branches in the complement $\mathcal{Z} \setminus \bar{\mathcal{Z}}$ for norators. Again, we have $\mathcal{V} = \mathcal{V}^\infty \cap \mathcal{V}^0$ and therefore $\mathcal{L} = \mathcal{L}^\infty \cap \mathcal{V}^0$. As in the introductory example we parameterize $\mathcal{L}^\infty$ and search it for the intersection points with $\mathcal{V}^0$. The above source replacements deliver new networks $\mathcal{N}^x = (G, \mathcal{V}^x)$ with $\mathcal{V}^x := \{(v,i) \in \mathcal{V}^\infty | \forall b \in \bar{\mathcal{Z}}_V : v_b = x_b, \forall b \in \bar{\mathcal{Z}}_I : i_b = x_b\}$ for each prescribed source value assignment $x \in \mathbb{R}^{\bar{\mathcal{Z}}}$. By Nielsen and Willson the networks $\mathcal{N}^x$ have unique solutions and the map $x \in \mathbb{R}^{\bar{\mathcal{Z}}} \mapsto (u,i) \in \mathcal{L}^x$ parameterizes $\mathcal{L}^\infty$. In most cases it is possible to find a reasonable bounded parameter set

[4] In the case that the power supply voltage is considerably higher than the threshold voltage of a basis-emitter diode one can take the Ebers-Moll equations into consideration to estimate narrow bounds for the homotopy parameter.

$X \subset \mathbb{R}^{\bar{\mathcal{Z}}}$ such that $\mathcal{L}^X := \cup_{x \in X} \mathcal{L}^x$ covers all the solutions of $\mathcal{N}$. In the case of two replaced branches the set $\mathcal{L}^X$ can be computed by means of a parameterized dc-sweep of `pspice` and the intersection points with $\mathcal{V}^0$ can be found via the graphic program `gnuplot`. An example follows in section 4.

Since the computational effort grows exponentially with the number of replaced branches it is quite desirable to stick to the case of one replaced branch even if uniqueness cannot be ensured for that case. But then one has to be aware that $\mathcal{L}^\infty$ can consist of several components which may even have turning points. Problems with turning points can be avoided if one parameterizes the curves by arc length via a path-following algorithm. Because of lack of space we can only give a simplified sketch here (for a more detailed presentation see [3,5,9]). The path following algorithm is realized with a transient analysis of `spice` applied to an auxiliary dynamical network $\widetilde{\mathcal{N}} = (\mathcal{G}, \widetilde{\mathcal{V}})$. We use here C^1-time functions $u, i \in \mathrm{C}^1(T, \mathbb{R}^{\mathcal{Z}})$ of voltage- and current assignments defined on some time interval $T = [0, t_{\mathrm{end}}]$ and introduce $\widetilde{\mathcal{S}} := \mathrm{C}^1(T, \mathbb{R}^{\mathcal{Z}}) \times \mathrm{C}^1(T, \mathbb{R}^{\mathcal{Z}})$, Kirchhoff's set $\widetilde{\mathcal{H}} := \{(u,i) \in \widetilde{\mathcal{S}} | \forall t \in T : (u(t), i(t)) \in \mathcal{H}\}$, the behavioral relation $\widetilde{\mathcal{V}} := \{ (u,i) \in \widetilde{\mathcal{S}} \,|\, \forall t \in T : (u(t), i(t)) \in \mathcal{V}^\infty, \| \mathrm{D}_t\, u(t) \|^2 + \| \mathrm{D}_t\, i(t) \|^2 = 1\}$ with the time derivative D_t and an appropriate norm $\| \bullet \|$ on $\mathbb{R}^{\mathcal{Z}}$, and finally the solution set $\widetilde{\mathcal{L}} = \widetilde{\mathcal{V}} \cap \widetilde{\mathcal{H}}$. Obviously, we obtain the identity

$$\widetilde{\mathcal{L}} = \{(u,i) \in \widetilde{\mathcal{S}} | \forall t \in T : (u(t), i(t)) \in \mathcal{L}^\infty, \| \mathrm{D}_t\, u(t) \|^2 + \| \mathrm{D}_t\, i(t) \|^2 = 1\}.$$

The additional behavioral equation $\| \mathrm{D}_t\, u(t) \|^2 + \| \mathrm{D}_t\, i(t) \|^2 = 1$ forces, that the curves $t \in T \mapsto (u(t), i(t))$ in $\mathcal{L}^\infty$ are traced with constant speed and therefore are parameterized by some equivalent of arc length. This equation can be described by a `spice` netlist with entries for capacitors and controlled sources. The set $\mathcal{L}^T := \{(u(t), i(t)) \in \mathcal{S} | (u,i) \in \widetilde{\mathcal{L}}, t \in T\}$ which consists of traces of the curves $t \in T \mapsto (u(t), i(t))$ is a subset of $\mathcal{L}^\infty$ and can be used as a replacement for $\mathcal{L}^X$.

4 Examples

• Analogous to the introductory example, the dpc-method is applied to the network in figure 6 and the associated homotopy path is computed by a dc-sweep of `spice`. Therefore, a family of networks $\mathcal{N}^x$ is constructed by exchanging the voltage source for a current source with source current $x \in X$ (replacing the behavioral equation $v_a = 5$ with $i_a = x$). The networks $\mathcal{N}^x$ have unique solutions since they are not reducible to the feedback structure. The bounds of the parameter interval $X = [0, 0.011]$ can easily be estimated by the cutset equation for the branches R_1, R_2, R_3, a and by the fact that no branch voltage exceeds the value 5. From the `spice`-computed dc-sweep in figure 7 one sees that the behavioral equation $v_a = 5$ of $\mathcal{N}$ is satisfied for five parameter values x (which equal i_a). Therefore $\mathcal{N}$ exhibits five dc-operating points. This example suggests that sometimes it may be useful to use our method instead of the usual voltage source stepping for global dc-analysis.

• Next we sketch the transfer-characteristic method from [8]. Consider again

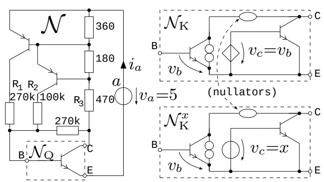


Figure 6

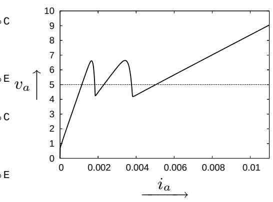


Figure 7

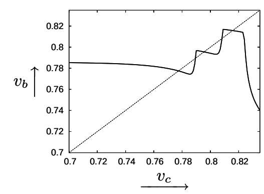


Figure 8

the network $\mathcal{N}$ in figure 6 but now with the transistor $\mathcal{N}_Q$ substituted by the terminal equivalent subnetwork $\mathcal{N}_{\mathrm{K}}$ (such a kind of substitution is due to Kronenberg [1]). For a global dc-analysis a family $(\mathcal{N}^x)_{x\in X}$ of networks is constructed. In each $\mathcal{N}^x$ the controlled source is replaced by an independent voltage source with source voltage x (see the corresponding subnetwork $\mathcal{N}_{\mathrm{K}}^x$ in figure 6). Uniqueness of the solution of $\mathcal{N}^x$ can be proven by the methods given in [7]. The parameter interval $X = [0, 0.84]$ is found with the help of the estimation for the current of the power supply (see above) and the Ebers-Moll equations. From the result of a `spice` dc-sweep (see figure 8 for the relevant section of it) one reads off the parameter values x (equal to v_c) which fulfill the behavioral equation $v_b = v_c$ of the controlled source. These parameter values correspond to the solutions of $\mathcal{N}$ (cf. [8] for details).

• At least two voltage sources have to be inserted into the network $\mathcal{N}$ of figure 9 to break all feedback structures. With the aid of a parametric dc-sweep of `pspice` it is possible to compute the solutions of the resulting networks $\mathcal{N}_{a,b}^x$ (see figure 10) in dependency of the source voltages $x_a, x_b \in [0, 5]$. The

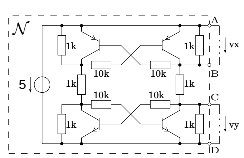


Figure 9

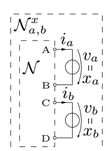


Figure 10

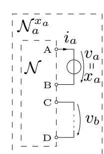


Figure 11

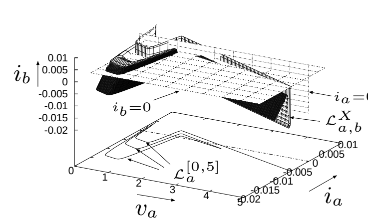


Figure 12

bounds of the two-dimensional parameter set $X := [0, 5]^{\{a,b\}}$ are induced by the source voltage of the power supply of $\mathcal{N}$. The set $\mathcal{L}_{a,b}^{\infty}$ of all solutions of the networks $\mathcal{N}_{a,b}^x$ ($x \in \mathbb{R}^{\{a,b\}}$) is a two-dimensional manifold which can be parametrized by the source voltages x_a and x_b. The projection of the relevant part $\mathcal{L}_{a,b}^X \subset \mathcal{L}_{a,b}^{\infty}$ onto the v_a-, i_a- and i_b-components is depicted in figure 12. The points of $\mathcal{L}^X_{a,b}$ satisfying $i_a = 0$ and $i_b = 0$ are the solutions of $\mathcal{N}$. They are determined in two steps. At first the set $\mathcal{L}^{[0,5]}_a \subset \mathcal{L}^X_{a,b}$ of points with $i_b = 0$ is computed via a contour plot of the well-known freely available program `gnuplot`. This set is the union of the solution sets $\mathcal{L}^{x_a}_a$ $(x_a \in [0,5])$ of networks $\mathcal{N}^{x_a}_a$ with only one inserted voltage source at branch a (see figure 11). The projection of $\mathcal{L}^{[0,5]}_a$ onto the (v_a, i_a)-plane is also shown in figure 12. From this projection the parameters v_a with $i_a = 0$, i.e. the v_a-values corresponding to solutions of $\mathcal{N}$, can be read off. The corresponding v_b values are similarly determined. In this way one obtains the parameter values v_a and v_b for the nine dc-operating points of the network $\mathcal{N}$. Figure 12 shows that a dc-analysis of the networks $\mathcal{N}^{x_a}_a$ (see figure 11) with x_a as the sweep parameter will not succeed since $\mathcal{L}^\infty_a$ cannot be parameterized by x_a.

• The last example shows the application of the dpc-method to a somewhat larger transistor network. The circuit in figure 13 represents a simple oper-

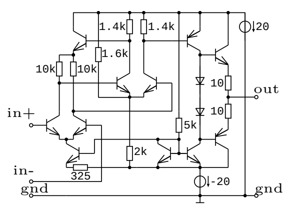


Figure 13

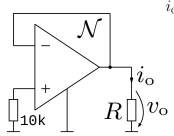


Figure 14

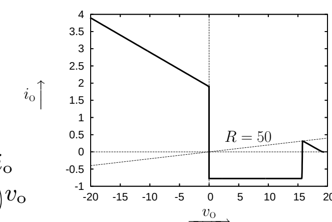


Figure 15

ational amplifier which models the latch-up effect of the μA 709 (see [2]). This amplifier is applied in network $\mathcal{N}$ (see figure 14) as a voltage follower with input connected to ground by a 10k resistor. For the computation of dc-operating points of this transistor network the load R has been replaced by a voltage source and a dc-analysis was carried out with the source voltage as the dc-sweep parameter. In the sense of the proof above this is interpreted as exchanging the load for a norator and then covering the v-i-relation of the resulting network with the v-i-relations of a family of networks where the norator is replaced with voltage sources. The i_o-component of the corresponding solution is shown as a bold curve in figure 15. The light straight line in figure 15 is the v-i-characteristic of a resistor with value 50. If the load resistance is larger than 50 then the circuit $\mathcal{N}$ has at least three dc-solutions, i.e. it exhibits the latch-up effect.

Note that we did not break all feedback structures in network $\mathcal{N}$ by inserting the voltage source. Therefore the parameterization of the solution set $\mathcal{L}^\infty$ by v_o is not necessarily unique and it is possible that there exist some other solution components of $\mathcal{N}^\infty$ which have been skipped by the dc-analysis (cf. previous example). In particular, vertical line segments in a `spice`-computed dc-plot as they occur in figure 15 can indicate that the solution manifold consists of more than one component. It may be that such a line segment does not belong to the solution manifold $\mathcal{L}^\infty$ but connects two separate components of $\mathcal{L}^\infty$. In order to exclude this case, the characteristic in figure 15 has been verified with the help of the curve tracing algorithm by J. Haase which can also be implemented as a `spice` netlist. This last example shows that the dpc-method can be useful for detecting multiple dc-solutions even if well defined parameterization is not ensured.

5 Conclusions

With the help of homotopies, global search for all dc-operating points of a network becomes global search of a low-dimensional parameter space. Interesting projects for larger networks are **(1st)** an effective topological algorithm for the highly complex task to place a minimal number of independent sources needed to break all feedback structures, **(2nd)** an algorithm for the global dc-analysis basing on the proposed homotopy method that can compete with existing global algorithms.

We thank the anonymous reviewers very much for their recommendations.

References

1. Kronenberg, L., Trajković, Lj., and Mathis, W.: Analysis of feedback structures and their effect on multiple dc-operating points. *Proc. ECCTD'99*, Stresa, Italy, Aug. 1999, pp. 683–686.
2. Widlar, R. J.: Design Techniques for Monolithic Operational Amplifiers. IEEE Journal of Solid-State Circuits, vol. SC-4, No. 4, August 1969
3. Haase, J.: Computation of transfer characteristics of multivalued resistive non-linear networks. Proc. SSCT82, Part: Short Communications. (1982) 286–272
4. Nielsen, R. O., Willson, A. N.: A Fundamental Result Concerning the Topology of Transistor Circuits with Multiple Equilibria. Proceedings of the IEEE on Circuits and Systems. 68 (1980) 196–208
5. Ushida, A., Chua, L. O.: Tracing solution curves of non-linear equations with sharp turning points. International Journal of Circuit Theory and Applications. 12 (1984) 1–22
6. Willson, A. N.: The no-gain property for networks containing three-terminal elements. IEEE Trans. Circuits and Systems. CAS-22 (1975) 678–687
7. Hasler, M., Neirynck, J.: Nonlinear Circuits. Artech House, inc. Norwood, 1986.
8. Reibiger, A., Mathis, W., Nähring, T., Trajković, Lj., Kronenberg, L.: Mathematical Foundations of the TC-Method for Computing Multiple DC-Operating Points. XI. ISTET'01 preprints CD-ROM, Linz–Austria, 2001.
9. Nähring, T., Reibiger, A.: Beiträge zur Arbeitspunktberechnung resistiver Netzwerke. Kleinheubacher Berichte, 45 (2001) 262–265